

include a material substantially equal or similar to those of the adhesion layers A11 and A12 described above with reference to FIGS. 18 and 19. In addition, the interconnect portion 3100 may further include at least one third insulating layer and at least one third electrode portion on the second insulating layer 350. In addition, the uppermost layer of the interconnect portion 3100 may be protected by a passivation layer. The specific configuration of the interconnect portion 3100 illustrated in FIG. 26 is merely a non-limiting example. In an actual device, the interconnect portion 3100 may have a more complicated configuration than the illustrated configuration and may be variously changed.

[0144] Methods of manufacturing the above-described diffusion barrier layer, the multilayer structure including the diffusion barrier layer, and the electric device (semiconductor device) including the multilayer structure will be described below.

[0145] The diffusion barrier layers B10, B11, and B12 according to example embodiments may be formed in a range from room temperature to about 1,000° C. of a metal precursor including a metal element and a chalcogen source including a chalcogen element. Although the diffusion barrier layers B10, B11, and B12 may be formed by a chemical vapor deposition (CVD) process, the diffusion barrier layers B10, B11, and B12 may also be formed by an atomic layer deposition (ALD) process or other processes. In addition, although a vapor precursor may be used during the forming of the diffusion barrier layers B10, B11, and B12, a liquid or solid precursor may also be used. Various methods that are usable for forming 2D material layers may be applied to form the diffusion barrier layers B10, B11, and B12. Therefore, the diffusion barrier layers B10, B11, and B12 may be easily formed. In this respect, the diffusion barrier layers B10, B11, and B12 have excellent process suitability. Since a method of forming structures of electronic elements except for the diffusion barrier layers B10, B11, and B12 is well known, a detail description thereof will be omitted.

[0146] Additionally, since the diffusion barrier layers B10, B11, and B12 according to example embodiments may be formed using 2D materials, the diffusion barrier layers B10, B11, and B12 may have flexible characteristics. Therefore, the diffusion barrier layers B10, B11, and B12 and the multilayer structures including the same may be easily applied to various flexible devices.

[0147] It should be understood that example embodiments described herein should be considered in a descriptive sense only and not for purposes of limitation. Descriptions of features or aspects within each device or method according to example embodiments should typically be considered as available for other similar features or aspects in other devices or methods according to example embodiments. It will be understood by those of ordinary skill in the art that the configurations of the diffusion barrier layer, the multilayer structure including the diffusion barrier layer, and the electronic device (semiconductor device) including the multilayer structure described above with reference to FIGS. 1 to 26 may be variously modified. Specifically, the diffusion barrier layer may have a thickness of about 10 nm or more, and the diffusion barrier layer may be disposed between two different conductive layers (metal layers or metallic material layers) and serve to limit or prevent a material from moving between the two different conductive layers. In addition, the

configuration of the electronic device (semiconductor device) to which the diffusion barrier layer is applied may also be variously modified.

[0148] While some example embodiments have been particularly shown and described, it will be understood by one of ordinary skill in the art that variations in form and detail may be made therein without departing from the spirit and scope of the claims.

What is claimed is:

1. A multilayer structure comprising:

- a first material layer;
- a second material layer connected to the first material layer, the second material layer being spaced apart from the first material layer; and
- a diffusion barrier layer between the first material layer and the second material layer, the diffusion barrier layer including a non-graphene-based two-dimensional (2D) material.

2. The multilayer structure of claim 1, wherein the 2D material includes a metal chalcogenide-based material having a 2D crystal structure.

3. The multilayer structure of claim 2, wherein

the metal chalcogenide-based material includes at least one metal element selected from the group consisting of molybdenum (Mo), tungsten (W), niobium (Nb), vanadium (V), tantalum (Ta), titanium (Ti), zirconium (Zr), hafnium (Hf), technetium (Tc), rhenium (Re), ruthenium (Ru), cobalt (Co), palladium (Pd), platinum (Pt), copper (Cu), gallium (Ga), indium (In), tin (Sn), germanium (Ge), and lead (Pb),

and the metal chalcogenide-based material includes at least one chalcogen element selected from the group consisting of sulfur (S), selenium (Se), tellurium (Te), and oxygen (O).

4. The multilayer structure of claim 1, wherein the 2D material includes a transition metal dichalcogenide (TMDC).

5. The multilayer structure of claim 1, wherein the 2D material has a trigonal prismatic crystal structure or an octahedral crystal structure.

6. The multilayer structure of claim 1, wherein the diffusion barrier layer has a thickness of greater than 0 nm and less than or equal to about 5 nm.

7. The multilayer structure of claim 1, wherein the diffusion barrier layer has a thickness of greater than 0 nm and less than or equal to about 3 nm.

8. The multilayer structure of claim 1, wherein the diffusion barrier layer has a resistivity of about 10^{-4} Ω·cm to about 10^{-2} Ω·cm.

9. The multilayer structure of claim 1, wherein the diffusion barrier layer is doped with a dopant.

10. The multilayer structure of claim 1, wherein the first material layer includes an insulator, and the second material layer includes a conductor.

11. The multilayer structure of claim 1, wherein the first material layer includes a semiconductor, and the second material layer includes a conductor.

12. The multilayer structure of claim 1, further comprising:

- a conductor;
- an understructure; and
- an insulating material layer on the understructure, wherein